Notice of Allowability	Application No.	Applicant(s)	
	10/604,361	YANG ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the case filed 7/14/2003*.

2. ☒ The allowed claim(s) is/are *1-10*.

3. ☒ The drawings filed on *14 July 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

In claim 1, line 15, "masking" has been replaced with –is masking--, for grammatical correctness.

In claim 9, line 13, "masking" has been replaced with –is masking--, for grammatical correctness.

The following is an examiner's statement of reasons for allowance: the prior art, either singly or in combination, fails to anticipate or render obvious, the method including the limitations of depositing a protective dielectric layer over the semiconductor substrate, coating a patterning an etch array (EA) photoresist layer on the protective dielectric layer, so that the EA photoresist layer is masking the support region and a portion of the transition region, using the EA photoresist layer as an etching mask and etching the protective dielectric layer to expose the first pad nitride in the vertical transistor memory array region, using the protective dielectric layer to protect the second pad nitride in the support region and removing the first pad nitride in the vertical transistor memory array region to form recesses on the array active areas, forming spacers on walls of the recesses on the array active areas, depositing a dielectric layer covering the protective dielectric layer on the support region, the vertical

transistor memory array region, and the transition region and the dielectric layer filling the recesses, and performing CMP to polish the dielectric layer and the protective layer on the support region using the second pad nitride as a polishing stop layer in combination with the other limitations of independent claim 1.

Further, the prior art, either singly or in combination, fails to anticipate or render obvious, the method including the limitations of depositing a protective dielectric layer over the semiconductor substrate, coating a patterning an etch array (EA) photoresist layer on the protective dielectric layer, so that the EA photoresist layer is masking the support region and a portion of the transition region, using the EA photoresist layer as an etching mask and etching the protective dielectric layer to expose the first pad nitride in the vertical transistor memory array region, removing the first pad nitride in the vertical transistor memory array region to form recesses on the array active areas, depositing a dielectric layer covering the protective dielectric layer on the support region, the vertical transistor memory array region, and the transition region and the dielectric layer filling the recesses, performing CMP to polish the dielectric layer and the protective layer on the support region using the second pad nitride as a polishing stop layer, depositing a silicon layer over the semiconductor substrate, coating and patterning an etch support (ES) photoresist layer on the silicon layer, the ES photoresist layer masking the vertical transistor memory array region and a portion of the transition region, and etching the silicon layer using the ES photoresist layer as a hard mask to define an array etch mask, in combination with the other limitations of independent claim 9.

Beintner et al. teach a similar method, but do not disclose the method of coating a patterning an etch array (EA) photoresist layer on the protective dielectric layer, so that the EA photoresist layer is masking the support region and a portion of the transition region, and using the EA photoresist layer as an etching mask and etching the protective dielectric layer to expose the first pad nitride in the vertical transistor memory array region. Beintner et al. do disclose the method of utilizing a masking process, but do not disclose the steps of using the photoresist. As can be seen in Figure 5, Beintner et al. do not cover the transition region during masking. Finally, Beintner et al. do not disclose removing the first pad nitride in the vertical transistor memory array region to form recesses on the array active area and forming spacers on walls of the recesses on the array active area. Beintner et al. do disclose the method of forming spacers on recesses, but not the recesses that are created by removing the pad nitride.

With respect to claim 9, Beintner et al. also do not disclose the method of depositing a silicon layer over the semiconductor substrate, coating a patterning an etch support (ES) photoresist layer on the silicon layer, the ES photoresist layer masking the vertical transistor memory array region and a portion of the transition region, and etching the silicon layer using the ES photoresist layer as a hard mask to define an array etch mask.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Patent Examiner
Art Unit 2812

jmk